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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,239	CHOI, JONG-HYUN	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,10-13,15-24,26,28-33 and 35-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,10-13,15-24,26,32,33 and 35-37* is/are rejected.

7)☒ Claim(s) *28-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Translation

The amendment and translation of the foreign priority document submitted on Apr 23, 2007 were reviewed and considered with the following results:

The amended claims overcame the objections to claims 1-3, 5-6, 15-16, and 35 as described on page 4 of the previous Office Action, wherein those objections have now been withdrawn.

The amended claims, and/or related arguments, overcame the rejections of claims 1-3, 5-6, 10-13, 15-18, 28-33, and 35-37 described on pages 5-6 of the previous Office Action. Although those rejections have been withdrawn, amended claim 10 had new rejections created. These are described later under the appropriate section.

The English translation of the foreign priority document overcame all of the prior art rejections cited in the previous Office Action. Therefore, the following rejections have been withdrawn: 1) 1-3, 5-6, 10-13, 15-18, 32-33, and 35-37, under 35 U.S.C. 103(a), with respect to Hardee/Origasa; and 2) claims 1-3, 5-6, 10-13, 15-16, 19-24, 26, 32-33, and 35-37 under 35 U.S.C. 103(a), Origasa/Wright et al. The Origasa does not beat the Feb 10, 2003 foreign priority date, and therefore can no longer be used within a prior art rejection.

Although the prior art rejections from the previous Office Action have now been withdrawn, the claims are now rejected citing another reference that shows/teaches the relationship between a row address signal and a voltage (or level) translator/shifter, wherein that reference's date is prior to the foreign priority date. These rejections are described later under the appropriate section.

Due to these new rejections, with respect to the newly cited secondary reference, this Office Action is **NON-FINAL**.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10-13 and 15-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not understood why the drain/source limitations of all the transistors within claim 10 were changed. Although the drain/source of the first transistor now corresponds to the applicant's figures, the drain/source connections of the second and third transistors are now reversed, and are thus misleading. For example, which of the applicant's figures actually show the source of the second transistor coupled to the output terminal, while the drain of the third transistor is coupled to a ground voltage? Claims 11-13 and 15-18 carry over the rejection of claim 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-6, 10-13, 15-18, 32-33, and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardee, cited previously, in view of Amanai, a reference found during the recent update search to obtain at least one example of a row address/level shift type circuit

with a date clearly prior to the present application's foreign priority date. One of ordinary skill in the art would understand that Fig. 1 of Hardee shows a level shifting type device for receiving an input signal alternating between 0V and VCC, and for effectively providing a corresponding output signal that will selectively alternate between 0V and VCCP. The device comprises first internal circuit 12, including first MOS transistor 12, operating at first voltage VCCP higher than power supply voltage VCC of the device (e.g. see column 1, lines 25-28); second internal circuit 16, including second MOS transistor 16, operating at second voltage VCC lower than first voltage VCCP; and restricting means 14, including third MOS transistor 14 with a thin gate insulation layer (i.e. THIN OXIDE) and operating at second voltage VCC, wherein restricting means 14 will restrict a voltage transmitted from first internal circuit 12 to second internal circuit 16 by applying the voltage from first internal circuit 12 to second internal circuit 16 through third MOS transistor 14. Although second MOS transistor 16 is controlled by the input signal alternating between VCC and 0V, this signal is neither clearly shown nor disclosed as being related to a row address signal in a memory device. However, one of ordinary skill in the art would understand Hardee's device would be capable of operating with a row address signal as its input signal. Column 1, lines 24-28 of Hardee disclose the device relates to memory devices which may require the higher voltage, and therefore could be used with a memory device and its related signals. Amanai shows and discloses a memory related device utilizing a row address signal and a level shifter. For example, Fig. 1 shows level shifter 15 controlled by a row address signal provided through gate 13. Therefore, it would have been obvious to one of ordinary skill in the art to supply second MOS transistor 16 of Hardee with a row address signal in a memory device, and/or to replace Amanai's level shifting type circuitry 15 with Hardee's device, wherein

second MOS transistor 16 would be controlled by at least one row address signal through Amanai's logic gate 13, rendering claim 1 obvious. The type of signal applied to Hardee's second MOS transistor would depend on what type of input signal is to be shifted to provide a higher "high" level output. Since first MOS transistor 12 has a thick gate insulation layer (i.e. THICK OXIDE), and second MOS transistor 16 has a thin gate insulation layer (i.e. THIN OXIDE), it would be obvious to one of ordinary skill in the art that the voltage transmitted from first internal circuit 12 to second internal circuit 16 would reduce an electric field applied to the gate insulation layer of second MOS transistor 16 since restricting means 14 functions at a resistance device that provides a voltage drop across it, thus rendering claim 2 obvious. Second voltage VCC is a power supply voltage that would be either an external power supply voltage, or an internal power supply voltage, for the device, and claim 3 is rendered obvious. It would have been obvious to one of ordinary skill in the art to couple an inverter to a connection node between the first and third MOS transistors (i.e. 12 and 14, respectively) of Hardee, wherein the inverter would drive a word line in the memory device, rendering claim 5 obvious. The inverter would provide an inverted version of the output signal from Hardee's circuit, if it was desired or required, and also provide one means for isolating the word line from Hardee's device. It would be obvious to one of ordinary skill in the art that the inverter include PMOS and NMOS transistors operating at a third voltage VCCP (of Hardee) higher than power supply voltage VCC, wherein each transistor would have a thick gate insulation layer. This renders claim 6 obvious. The inverter would include PMOS and NMOS transistors to closely correspond to the MOS transistors in Hardee's device, thus allowing all the transistors to have similar fabrication processes and operating characteristics. The inverter transistors will have a thick oxide to

prevent their breakdown, since they operate at the higher voltage VCCP. Interpreting Hardee's Fig. 1 circuit in a slightly different manner, the device comprises an output terminal (i.e. the unlabeled connection between transistors 12 and 14) selectively receiving high voltage VCCP higher than power supply voltage VCC of the device; first transistor 12 having a drain coupled to the output terminal, a source coupled to high voltage VCCP, a gate coupled to a first input signal that selectively alternates between 0V and VCCP, and a thick gate insulation layer (i.e. THICK OXIDE); second transistor 14 having a drain coupled to the output terminal, a gate coupled to low voltage VCC lower than high voltage VCCP, and a thin gate insulation layer (i.e. THIN OXIDE); and third transistor 16 having a drain coupled to the source of second transistor 14, a source coupled to a ground voltage, a gate coupled to a second input signal selectively alternating between 0V and VCC, and a thin gate insulation layer (i.e. THIN OXIDE). For the same type of reasoning as described above with respect to claim 1, the second input signal applied to the gate of third transistor 16 is capable of being, or with respect to Amanai can be, a row address signal from a memory device. Therefore, claim 10 is rendered obvious. Since second voltage VCC is the power supply voltage, which is an external power supply voltage, or an internal power supply voltage, of the device, claim 11 is also rendered obvious. One of ordinary skill in the art would understand that 0V is a low level corresponding to the ground voltage. Therefore, the first input signal is selectable as one of a high level of high voltage VCCP and a low level of ground; and the second input signal is selectable as one of a high level of low voltage VCC and a low level of ground, rendering claims 12-13 obvious. Claims 15-16 are rendered obvious for the same reasoning as previously described above with claims 5-6, respectively. Hardee discloses that any number of NMOS transistors can be coupled in series to

configure the switching circuit into a NAND logic configuration (e.g. see column 4, lines 29-36 and Fig. 4B). Therefore, it would have been obvious to one of ordinary skill in the art to couple a fourth transistor between third transistor 16 of Hardee and ground. This fourth transistor would have a thin gate insulation layer because it is related to the lower voltages within the device, not high voltage VCCP. Therefore, claim 17 is rendered obvious. The fourth transistor would provide another means for dropping voltage, thus helping to distribute the total voltage drop between the output terminal and ground across more transistors. Also, if the fourth transistor is used as part of a NAND logic configuration, it is capable of receiving a block selecting signal from the memory device, rendering obvious claim 18. Configured as NAND logic, the device will provide a low output signal only when the second input signal, and the block selecting signal, allow the third and fourth transistors to conduct. This will help ensure that the device will generate a low only when these specific conditions are met, and only when a low output signal is actually desired. By re-identifying the restricting means of claim 1 as an interface circuit, claims 32-33 and 35 are rendered obvious for the same type of reasoning as previously described with respect to claims 1-2. Since third MOS transistor 14 functions as a resistance device, one of ordinary skill in the art would know that it prevents first voltage VCCP from being directly applied to the drain of second MOS transistor 16, thus enabling it to have the thin gate insulation layer, and reducing the gate-drain voltage of second MOS transistor 16 to alleviate the electric field applied to the gate insulation layer of second MOS transistor 16. This knowledge renders respective claims 36 and 37 obvious.

Claims 1-3, 5-6, 10-13, 15-16, 19-24, 26, 32-33, and 35-37 are rejected under 35 U.S.C. 103(a) as being Wright et al. (Wright), cited in the previous Office Action, in view of

Amanai, a reference previously cited above. Wright shows a semiconductor integrated circuit device in Fig. 2 comprising level shifter 200 comprising six MOS transistors 202-212 and inverter 214. This basic structure corresponds to transistors MN11-MN12, MN9-MN10, and MP5-MP6 and inverter INV2, respectively shown in the applicant's Fig. 4. Therefore, one of ordinary skill in the art would understand Wright's configuration has a device comprising first internal circuit 212, including first MOS transistor 212, operating at first voltage VIO higher than power supply voltage VCORE of the device (e.g. see column 1, lines 28-32 and 48-50); second internal circuit 204, including second MOS transistor 204, operating at second voltage VCORE (i.e. inverted VIN, on line 224, will have VCORE as its high logic level) lower than first voltage VIO; and restricting means 208, including third MOS transistor 208 that can have a relatively thin gate insulation layer (e.g. see column 4, line 17-19, wherein a medium gate oxide is relatively thinner than a thick gate oxide) and operating at second voltage VCORE, wherein one of ordinary skill in the art will know restricting means 208 will restrict a voltage transmitted from first internal circuit 212 to second internal circuit 204 by applying the voltage from first internal circuit 212 to second internal circuit 204 through third MOS transistor 208. Second MOS transistor 204 is controlled by the inverted input signal VIN. However, VIN is neither clearly shown nor disclosed as a row address signal. Fig. 1 of Amanai shows level shifter 15 that corresponds to Wright's Fig. 1, wherein Wright modified Fig. 1 to obtain the level shifter shown in Wright's Fig. 2. Amanai's level shifter 15 is controlled with respect to a row address signal supplied through logic gate 13, and it would have been obvious to one of ordinary skill in the art to effectively supply a row address signal as VIN to Wright's circuit, rendering claim 1 obvious. For example, the use of Wright's circuit in a memory, for level shifting a row address signal, is

one type of intended use one of ordinary skill in the art would understand. Since first MOS transistor 212 has a thick gate insulation layer (i.e. see column 4, lines 17-18), and second MOS transistor 204 has a relatively thin gate insulation layer (i.e. see column 4, line 4), it would be obvious to one of ordinary skill in the art that the voltage transmitted from first internal circuit 212 to second internal circuit 204 would reduce an electric field applied to the gate insulation layer of second MOS transistor 204 since restricting means 208 functions at a resistance device that provides a voltage drop across it, thus rendering claim 2 obvious. Second voltage VCORE is a power supply voltage that is an internal power supply voltage for the device (e.g. see column 1, line 48-50), and claim 3 is rendered obvious. It also would have been obvious to connect node 220 of Wright, between first/third MOS transistors 212/208 to an inverter that drives a WL of the memory device, rendering claim 5 obvious. The inverter would allow isolation between the level shifter and subsequent circuitry, and provide an inverted signal at the proper levels when necessary. The inverter would obviously include PMOS/NMOS transistors operating at a third voltage VIO higher than power supply voltage VCORE when transistor 212 is conducting, wherein each transistor of the inverter would have a thick gate insulation layer because of the higher voltage. This renders claim 6 obvious. The MOS transistors would allow the inverter to operate under the same operating characteristics of the MOS transistors within Wright's circuit. Also, when all of the transistors within a circuit are made from the same basic types of transistors (e.g. MOS or bipolar), fabrication is easier. Interpreting the Wright/Amanai configuration in a slightly different manner, the device comprises output terminal 220 selectively receiving high voltage VIO higher than power supply voltage VCORE; first transistor 212 having a drain coupled to output terminal VOUT, a source coupled to high voltage VIO, a gate coupled to a first

input signal (from the common connection between 210 and 206), and a thick gate insulation layer (i.e. thick gate oxide); second transistor 208 having a drain coupled to output terminal VOUT, a gate coupled to low voltage VCORE lower than high voltage VIO, and a relatively thin gate insulation layer (i.e. a medium gate oxide is thinner than a thick gate oxide); and third transistor 204 having a drain coupled to the source of second transistor 208, a source coupled to a ground voltage, a gate coupled to a second input signal (i.e. an inverted version of Wright's input signal VIN, which corresponds to the row address signal supplied via Amanai's logic gate 13 as previously described), and a thin gate insulation layer (i.e. thin gate oxide). For the same type of reasoning as described above with respect to claim 1, the second input signal applied to the gate of third transistor 204 effectively includes a row address signal from a memory device. Therefore, claim 10 is rendered obvious. Since second voltage VCORE is the power supply voltage that is an internal power supply voltage of the device, claim 11 is also rendered obvious. The first input signal, generated at the common connection between 210 and 206, is selectable as one of a high level of high voltage VIO when transistor 210 is conducting, and a low level of ground when transistor 202 is conducting, thus rendering claim 12 obvious. The second input signal, provided at the output of Wright's inverter 214, is selectable as one of a high level of low voltage VCORE and a low level of ground, rendering claim 13 obvious. Claims 15-16 are rendered obvious for the same reasoning as previously described with respect to claims 5-6. In still another interpretation of the Wright/Amanai configuration, the device comprises power terminal 222 receiving high voltage VIO higher than power supply voltage VCORE of the device (e.g. see related column 1, lines 31-54); first MOS transistor 210 coupled between the power terminal and a first internal node (i.e. unlabeled connection between 210 and 206); second MOS

transistor 212 coupled between the power terminal and second internal node 220; third MOS transistor 206 coupled between the first internal node and a third internal node (i.e. unlabeled connection between 206 and 202); fourth MOS transistor 208 coupled between second internal node 220 and a fourth internal node (i.e. unlabeled connection between 208 and 204); fifth MOS transistor 202 coupled between the third internal node and a ground voltage, and controlled by first input signal VIN; and sixth MOS transistor 204 coupled between the fourth internal node and the ground voltage, and controlled by an inverted version of first input signal VIN. It would have been obvious that first input signal VIN effectively includes row address signal and a block selecting signal through Amanai's logic gate 13. Wright discloses that first/second MOS transistors 210/212 have a relatively thick gate insulation layer (e.g. see "thick gate oxide" on column 4, lines 17-18); third/fourth MOS transistors 206/204 can have a relatively thin gate insulation layer (e.g. see "medium gate oxide" on column 4, lines 18-19); and fifth/sixth MOS transistors 202/204 have a relatively thin gate insulation layer (e.g. see "thin gate oxide" on column 4, line 4), thus rendering claims 19-20 obvious. The replacement of Wright's input VIN with Amanai's row address/logic gate related input replaces one known type of input with another (e.g. one known type of intended use). Power supply voltage VCORE is an internal power supply voltage of the device (e.g. see column 1, lines 48-50), rendering claim 21 obvious. Since first MOS transistor 210 and second MOS transistor 212 are controlled by a voltage of the second and first internal nodes, respectively, claim 22 is rendered obvious. The gates of third/fourth MOS transistors 206/208 are each coupled to low voltage VCORE, which is lower than high voltage VIO, and an internal power supply voltage of the device as previously described, thus rendering claims 23-24 obvious. With the positive and negative power supply

terminals of inverter 214 connected to VCORE/ground, respectively, the first input signal and its inverted version are understood to be selectable, and will have one of a high level of low voltage VCORE and a low level of ground voltage, rendering obvious claim 26. By re-identifying the restricting means of claim 1 as an interface circuit, claims 32-33 and 35 are rendered obvious for the same type of reasoning as previously described with respect to claims 1-2. Since third MOS transistor 208 functions as a resistance device, one of ordinary skill in the art would know that it prevents first voltage VIO from being directly applied to the drain of second MOS transistor 204, thus enabling it to have the thin gate insulation layer, and reducing the gate-drain voltage of second MOS transistor 204 to alleviate the electric field applied to the gate insulation layer of second MOS transistor 204. This knowledge renders respective claims 36 and 37 obvious.

No claim is allowable as presently written.

Claims 4, 7-9, 14, 25, 27, and 34 have been cancelled.

Allowable Subject Matter

Claims 28-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the first internal node is coupled to the row decoder and driver block of the memory device, wherein that block selectively drives word lines of the memory device in response to row address signals, as recited within claim 28, upon which claims 29-31 depend.

Response to Arguments/Foreign Priority Translation

The applicant's foreign translation overcame the previous prior art rejections described in the previous Office Action since the reference of Origasa (one known example of a level shifter related to a memory device and row address signal) did not have a date that satisfactorily beat the date of the foreign priority document. Therefore, all the prior art rejections cited in the previous Office Action have been withdrawn. However, upon further consideration, the claims are now rejected in view of the secondary reference by Amanai, which was issued on Oct 3, 2000. Those rejections are described above within their appropriate section.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed limitations related to row address signals, level shifters, and memory devices. Although not cited within any of the prior art references above, each of these references clearly shows the well known use of a level shifter similar to Wright's Fig. 1, wherein each of these references was issued prior to Feb, 10, 2003 (the foreign priority date). For some examples of a row address signal input being effectively supplied into a level shifter, see Umezawa et al (row address signal Ai and level shifter 30 in each of Figs. 13 and 18) and Matsumoto et al. (the level shifter of Fig. 5 receiving row address signal A). Therefore, each of these references should be carefully reviewed and considered, since they clearly show and teach the well known concept of using a level shifter for shifting the level of at least a row address signal by a level shifter similar to Wright's basic four transistor level shifter 100 (Fig. 1), and its corresponding six transistor level shifter 200 (Fig. 2) that comprises thick and thin film transistors. The references are important because they show/disclose the concept was known prior to the applicant's Feb 10, 2003 date.

Due to the new rejections with respect to the newly cited secondary reference, this Office Action is **NON-FINAL**.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Drew Richards, can be reached on (571) 272-1736.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

22 July 2007

/Kenneth Wells/
Kenneth B. Wells
Primary Examiner